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| 09/523,990 | 03/13/2000 | Mou-Shiung Lin | MEG99-005 | 6138 |

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SAILE ACKERMAN LLC
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

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| EXAMINER |
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WALSH, DANIEL I

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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|------------------------------|--------------------------------------|-----------------------------------|--|
| Office Action Summary | Application No. 09/523,990 | Applicant(s) LIN ET AL. | |
| | Examiner DANIEL WALSH | Art Unit 2887 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 44, 48, 49 and 60-68 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 44, 48, 49 and 60-68 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Receipt is acknowledged of the Amendment received on 2-6-09.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 44, 48, 49, and 60-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (US 6,476,499) in view of Hiromasa (JP362169448A), as cited in a previous Office Action.

Hikita et al. teaches (FIG. 5, 16A+) a circuit component comprising a substrate, a semiconductor chip over a top surface of the substrate wherein the chip has a front surface facing the top surface of the substrate and a back surface opposite to the front surface and wherein said

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chip comprises multiple pads at the front surface; an identity of product directly on said back surface of the chip; multiple metal bumps between said multiple pads of said chip and said top surface of said substrate as bumps are used to bond the chips (1,2) to each other via electrodes (13,23) because it would have been obvious to use metal bumps/solder for conductivity, as is conventional in the art, such as for use between 13,23 of a first chip and a second chip/substrate.

Hikita et al. is silent to an optically transparent layer directly over said identity of product wherein said identity of product is visible through said optically transparent layer.

Hiromasa teaches a transparent resin through which identification information can be read (FIG. 1), broadly interpreted as an identity of a product. Though silent to a barcode being visible, it would have been obvious to one of ordinary skill in the art to use a barcode to provide machine readable indicia for reliability/accuracy. There mere claiming that the barcode is visible does not appear to effect the structure of the device, as the Examiner believes that information such as chip markings are capable of being read, as in indicia.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hikita et al. with those of Hiromasa in order to apply the teachings of transparent protective coatings over identification information

One would have been motivated to do this in order to protect/cover the information while still permitting it to be visible.

Re claim 48, Hikita et al. teaches a mold package (col 17, lines 55+). Though silent to an underfill between the front surface and a top surface of said substrate that encloses the metal bumps, the Examiner notes that is it well known and conventional in the art to

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underfill/encapsulate such packages (underfill material enclosing bumps and parts of the circuit/package) in order to seal/enclose/protect/strengthen elements of the device.

Re claim 49, though silent to balls on a bottom surface of said substrate, the Examiner notes that balls on a surface are an obvious expedient, well within the ordinary skill in the art, to effect connection between elements (pads/points of contact). The Examiner notes that balls/bumps are conventional to attach substrate together, as in flip chip/stacked chip arrangements, and therefore an obvious expedient to effect connection.

Re claims 61-68, the limitations have been discussed above. The Examiner notes that the barcode is taught as providing informational notations such as production lot number, model number, etc. Though silent to the identity of the manufacturer, the Examiner notes that the type of information contained in the printed matter is an obvious matter of design variation and is not functionally related to the substrate that it is on, and as such, is not patentable (see in re Gulack/Ngai). Merely specifying a type of information to be included is a matter of design variation, as merely conveying relevant desired information. Further, as such information claimed are just types of information notations as claimed, one would have been obvious to include such different notations to provide information to the user, for example; such relevant product information including information generally related to products such as product information, name, manufacturer, model number, etc., as known in the art.

4. Claims 48, 49, 60-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al./Hiromasa, as discussed above, in view of Flip Chip, as discussed in the previous Office Action.

The teachings of Hikita et al./Hiromasa have been discussed above.

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Hikita et al. /Hiromasa are silent to the underfill, balls on the bottom of the substrate, and solder bumps.

Flip Chip teaches such limitations (see lone drawing).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hikita et al. /Hiromasa with those of Flip Chip.

One would have been motivated to do this in order to use known techniques to produce predictable results, such as underfill/protection/covering of elements and connectivity (conductivity) between elements, as bumps/balls of metal/solder are known in the art to effect connectivity between elements, and underfills are known to provide protection/covering.

Re claims 61-68, the limitations have been discussed above. The Examiner notes that the barcode is taught as providing informational notations such as production lot number, model number, etc. Though silent to the identity of the manufacturer, the Examiner notes that the type of information contained in the printed matter is an obvious matter of design variation and is not functionally related to the substrate that it is on, and as such, is not patentable (see in re Gulack/Ngai). Merely specifying a type of information to be included is a matter of design variation, as merely conveying relevant desired information (additional). Further, as such information claimed are just types of information notations as claimed, one would have been obvious to include such different notations to provide additional information to the user, for example; such relevant product information including information generally related to products such as product information, name, manufacturer, model number, etc., as known in the art.

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5. Claims 44, 48, 49, 60, 62-64, and 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hyozo et al. (US 5,894,172) in view of Hiromasa, as discussed above, and Flip Chip, as discussed above.

Hyozo et al. teaches a chip with a front and back surface where the front surface is a bottom and the back surface is a top, and identity information (of product) directly on said back surface of the chip (FIG. 8). The Examiner notes that the type of information selected is a matter of design variation, not functionally related to the substrate and therefore is not patentable. The information 8 is interpreted as machine readable, motivated for increased efficiency and accuracy (machine reading).

Hyozo et al. is silent to the chip being a flip-chip/the structure of pads, bumps, solder, substrate, and underfill as claimed.

Flip Chip teaches such limitations, as discussed above.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hyozo et al. with those of Flip Chip.

One would have been motivated to do this to provide identification information on the chip (directly on the chip) that can be printed on the surface of the chip in various location, since no electronics circuit devices are connected on that surface of the chip. Applying such identification information to a flip-chip structure would enable known techniques to be provided on similar devices in a same way to produce predictable results, namely direct application of identification information.

Hyozo et al./Flip Chip are silent to a transparent encapsulant/coating.

Hiromasa teaches such limitations (as discussed above).

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At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hyozo et al./Flip Chip with those of Hiromasa in order to apply the teachings of transparent protective coatings over identification information.

One would have been motivated to do this to protect the information while still permitting it to be read (transparent).

Re claims 62-64 and 66-68, the limitations have been discussed above. The Examiner notes that the barcode is taught as providing informational notations such as production lot number, model number, etc. Though silent to the identity of the manufacturer, the Examiner notes that the type of information contained in the printed matter is an obvious matter of design variation and is not functionally related to the substrate that it is on, and as such, is not patentable (see in re Gulack/Ngai). Merely specifying a type of information to be included is a matter of design variation, as merely conveying relevant desired information (additional). Further, as such information claimed are just types of information notations as claimed, one would have been obvious to include such different notations to provide information to the user (additional), for example; such relevant product information including information generally related to products such as product information, name, manufacturer, model number, etc., as known in the art.

Though silent to a barcode being visible, it would have been obvious to one of ordinary skill in the art to use a barcode to provide machine readable indicia for reliability/accuracy. There mere claiming that the barcode is visible does not appear to effect the structure of the device, as the Examiner believes that information such as chip markings are capable of being read, as in indicia.

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6. Claims 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al./ Hiromasa, as discussed above, in view of Shumizu (JP405123237).

The teachings of Hikita et al./Hiromasa have been discussed above.

Hikita et al./Hiromasa is silent to a barcode visible through resin.

Shimizu teaches such limitations (CONSTITUTION).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hikita et al./Hiromasa with those of Shimizu.

One would have been motivated to do this to protect the barcode while still being readable/visible.

7. Claims 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al./ Hiromasa/Flip Chip, as discussed above, in view of Shumizu (JP405123237).

The teachings of Hikita et al./Hiromasa have been discussed above.

Hikita et al./Hiromasa/Flip Chip is silent to a barcode visible through resin.

Shimizu teaches such limitations (CONSTITUTION).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hikita et al./Hiromasa/Flip Chip with those of Shimizu.

One would have been motivated to do this to protect the barcode while still being readable/visible.

8. Claims 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hyozo et al./ Hiromasa/Clip Chip, as discussed above, in view of Shumizu (JP405123237).

The teachings of Hyozo et al./Hiromasa/Flip Chip have been discussed above.

Hyozo et al./Hiromasa/Flip Chip is silent to a barcode visible through resin.

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Shimizu teaches such limitations (CONSTITUTION).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hyozo et al./Hiromasa/Flip Chip with those of Shimizu.

One would have been motivated to do this to protect the barcode while still being readable/visible.

Response to Arguments

9. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

In response to the Applicants argument that the package material of Hiromasa is not transparent, the Examiner disagrees. The Examiner notes that Hiromasa teaches a transparent resin overlay to cover/protective markings/indicia. This transparent coating is being relied upon, and therefore the transparent coating (not the whole package) would cover the barcode.

The Examiner notes that claims do not require that the barcode is read, just that it is visible. As resin is transparent (disclosed) a barcode would be understood as visible (re the newly added claims).

Further, the Examiner notes that the claims regarding the different types of product related information, appear to be issues of printed matter, and therefore are not patentable. Merely claiming different types of information/printed matter that are not functionally related to the substrate is just a matter of design variation for providing different types of information (see in re Gulack/Ngai).

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Finally, the claimed 'substrate' is sufficiently vague to include a sheet such as a second chip, a carrier, etc., as part of the chip/circuit.

Response to Arguments

1. Applicant's arguments filed have been fully considered but they are not persuasive. The Examiner notes that Hiromasa teaches a transparent resin (4) that overlays the identification information beneath it, for protection. As Hikita et al. teaches identification information but not a coating for protection, the Examiner has noted that applying such a coating from the semiconductor package of Hiromasa to the semiconductor chip surface of Hikita et al. would have been obvious for protection of the notation/information, and such application being within the ordinary skill in the art. The Examiner notes that the package (2) of Hiromasa is not being relied upon to be transparent, and it is not envisioned that the package of the semiconductor chip of Hikita et al. would need to be transparent. The transparent resin which coats the identification information is the element relied upon for transparency, not the semiconductor chip/package.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WALSH whose telephone number is (571)272-2409. The examiner can normally be reached on M-F 9am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Paik can be reached on 571-272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DANIEL WALSH/
Primary Examiner, Art Unit 2887